

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
THIRD SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN (CS)

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks.

- | | Marks |
|--|-------|
| 1 Find the 9's and 10's complement of $(24579.12)_{10}$. | (3) |
| 2 Convert $(455)_{10}$ to base-4,8 and 16. | (3) |
| 3 Express the following functions as product of max-terms: | (3) |
| a) $F(X,Y,Z) = Y' + XZ' + XY'Z'$ b) $F(A,B,C) = C(A+B')(A'+B'+C')$ | |
| 4 Use Boolean Algebra to show that $A'BC' + AB'C' + AB'C + ABC' + ABC = A + BC'$ | (3) |

PART B

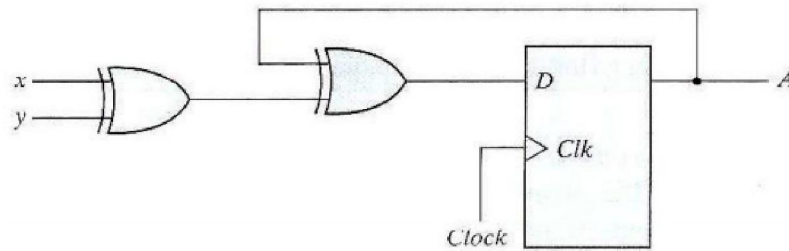
Answer any two full questions, each carries 9 marks.

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| 5 Simplify $F(A,B,C,D) = \Sigma(1,4,6,7,8,9,10,11,15)$ using Tabulation method and determine the prime implicants, essential prime implicants and the minimized Boolean expression. | (9) |
| 6 a) Subtract $(9F2C)_{16}$ from $(A96B)_{16}$ using 15's and 16's complement method. | (4) |
| b) Subtract 366 from 170 in BCD using 10's complement addition. | (3) |
| c) Perform $(417)_8 - (232)_8$ using 8's complement addition. | (2) |
| 7 a) Using K-map simplify the Boolean function F as Sum of Products using the don't care conditions d. | (4) |
| $F(w,x,y,z) = w'(x'y + x'y' + xyz) + x'z'(y+w)$
$d(w,x,y,z) = w'x(y'z + yz) + wyz$ | |
| b) Represent the following decimal numbers in signed 2's complement 8-bit numbers: i) +43 ii) -19 | (3) |
| c) Convert the decimal number 3.248×10^{-4} to IEEE 754 standard single precision floating point binary number. | (2) |

PART C

Answer all questions, each carries 3 marks.

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| 8 Differentiate combinational and sequential circuits. | (3) |
| 9 Given the block diagram of half-subtractor, implement a full-subtractor using half-subtractors. | (3) |
| 10 Write the excitation tables of SR, JK and T flip-flops. | (3) |
| 11 Given below is a sequential circuit using D flip-flop. Write the state table and draw a state diagram. | (3) |



PART D

Answer any two full questions, each carries 9 marks.

- 12 a) Design a sequential circuit with JK Flip flops to satisfy the following state equation. (5)
 $A(t+1) = A'B'CD + A'B'C + ACD + AC'D'$ $B(t+1) = A'C + CD' + A'BC'$
 $C(t+1) = B$ $D(t+1) = D'$
- b) Design and implement a decoder that decodes BCD digits (0000 to 1001). (4)
- 13 a) Design and implement a 2-bit magnitude comparator using 4X16 decoder. (5)
- b) Implement $f(A,B,C,D) = \Sigma(0,2,3,6,8,9,13,14)$ using 8 x 1 MUX. (4)
- 14 What is race around condition? Why does it occur? Discuss how master-slave flip-flop eliminates it. (9)

PART E

Answer any four full questions, each carries 10 marks.

- 15 a) Draw the logic diagram of a 4-bit Johnson counter and explain the working with a timing diagram. (8)
- b) Compare Ring counter and Johnson counter. (2)
- 16 a) Explain the working of 3-bit Universal Shift Register. (8)
- b) Give 2 applications of shift register. (2)
- 17 a) Design a combinational circuit using ROM that accepts a 3-bit binary number and generates output equal to the square of the input number. Use decoder of suitable size to implement ROM. (7)
- b) What size of ROM would it take to implement (3)
- A BCD adder/subtractor with a control input to select between the addition and subtraction.
 - A binary multiplier that multiplies two 4-bit numbers.
 - Dual 4-line to 1-line multiplexers with common selection inputs.
- 18 Design a synchronous counter using JK flip-flops to count the sequence 0,5,6,7,3,2 and then repeats. (10)
- 19 a) Compare static and dynamic RAMs. (3)
- b) A combinational circuit is defined by the functions: (7)
 $F1(A,B,C) = \Sigma(3,5,6,7)$ $F2 = \Sigma(0,2,4,7)$
 Implement the circuit with a PLA having 3 inputs, four product terms and 2 outputs.
- 20 With the help of a flowchart explain the addition/subtraction of binary numbers in sign magnitude form. (10)
