

Reg. No. _____ Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, JUNE 2017

Course Code: **EC206**

Course Name: **COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

PART A

Question No.1 is compulsory. Answer either Question No. 2 or Question No. 3.

1. (a) Illustrate the basic functional units of a digital computer and list the important functions of each unit. (4)
- (b) Explain briefly the principle of carry look-ahead addition. Draw the circuit diagram of 4 bit carry look-ahead adder with proper design. (7)
- (c) With the help of suitable examples, differentiate between R-type and I-type instructions in MIPS machine language. (4)
2. (a) Illustrate the IEEE standard format for single precision floating point numbers. (2)
- (b) Compute the delay of a 64-bit carry prefix adder, assuming that each 2-input gate delay is 200 ps. (4)
- (c) With a suitable circuit arrangement, explain n-bit binary multiplication. (6)
- (d) Design and implement a 4-bit equality comparator using gates. (3)
3. (a) Illustrate the format of J-type instructions in MIPS machine language. (2)
- (b) Write short notes on (i) MIPS register set (ii) Byte addressable memory. (7)
- (c) Assuming that the opcode 'addi' is represented by 8_{10} , register 'add' operation is represented by the function code 32_{10} , and the registers s_0 to s_7 are represented by 16_{10} to 23_{10} in MIPS machine language,
 - (i) Translate the following machine language code into MIPS assembly language: $0x2237FFF3$ (3)
 - (ii) Translate the following MIPS assembly code to MIPS machine language code in hexadecimal form: `add $s0, $s4, $s5` (3)

PART B

Question No.4 is compulsory. Answer either Question No. 5 or Question No. 6.

4. (a) With examples for each, explain the addressing modes available in MIPS. (7.5)

- (b) What is micro architecture? List the state elements of MIPS processor and their functions. (5)
- (c) Write a short note on performance analysis of computer systems. (2.5)
5. (a) With an illustration, briefly explain MIPS memory map. (5)
- (b) With a suitable diagram, explain the steps involved in executing a high level language program. (6)
- (c) With an example, briefly explain pseudo instructions in MIPS. (4)
6. (a) Differentiate between the three micro architectures for MIPS processor architecture. (3)
- (b) Derive the simplified expression for cycle time in a single cycle MIPS processor. If the cycle time in a single cycle processor is 1000 ps, compute the total execution time (in seconds) for a program with 10 lakh instructions. (7)
- (c) List the three main weaknesses of a single cycle processor. How are they eliminated in a multi cycle processor? (5)

PART C

Question No. 7 is compulsory. Answer either Question No. 8 or Question No. 9.

7. (a) With the help of a diagram, explain the concept of memory hierarchy. (4)
- (b) Write short notes on (i) SCSI (ii) USB (6)
- (c) With a diagram, explain address translation in virtual memory. (7)
- (d) Differentiate between the two different write policies in cache memory. (3)
8. (a) Explain in detail, the different modes of data transfer between the processor/memory and I/O devices in a computer system. (10)
- (b) What is a port? Differentiate between serial and parallel ports. (4)
- (c) With a circuit diagram, explain the working of a DRAM cell. (6)
9. (a) Briefly explain the concept of cache memory. What is hit rate? (3)
- (b) Discuss in detail, any two mapping methods in cache memory. (12)
- (c) Write short notes on (i) Replacement algorithms (ii) TLB (5)
