

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks

Marks

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|---|---|-----|
| 1 | a) Convert the following binary number into its equivalent gray code:
11010101 | (1) |
| | b) Convert the following gray code into its binary: 10101110 | (1) |
| | c) Perform the following arithmetic operation using 2's complement representation: 58 – 34 | (3) |
| 2 | Sensors are used to monitor the pressure and temperature of a chemical solution stored in a tank. The circuitry for each sensor produces a high voltage when a specified maximum value is exceeded. An alarm requiring a low voltage input must be activated when either the pressure or temperature is excessive. Design a circuit for this application. | (5) |
| 3 | Draw the circuit of a full adder and explain. | (5) |
| 4 | Distinguish between Sequential and combinational circuits. | (5) |
| 5 | Explain the design procedure of a synchronous counter without lock out. | (5) |
| 6 | Differentiate Moore and Mealy machines. Explain with examples. | (5) |
| 7 | Give the basic operation of a successive approximation ADC | (5) |
| 8 | Compare PAL, PLA and FPGA. | (5) |

PART B

Answer any two questions, each carries 10 marks

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| 9 | a) Find the standard sum of products (SOP) for the logic expression:
$F(A, B, C, D) = AB + \bar{A}\bar{B}\bar{D} + \bar{B}CD$ | (5) |
| | b) Use K-map to minimize the expression:
$F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 9, 10, 12, 13, 14, 15)$ | (5) |
| 10 | a) Design a three-bit odd parity detector circuit. | (5) |
| | b) Design the logic circuit for a BCD to decimal decoder. | (5) |
| 11 | Draw a neat diagram of TTL NAND gate and explain its operation. What is meant by sourcing and sinking? | (10) |

PART C

Answer any two questions, each carries 10 marks

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| 12 | Explain the operation of a Master slave JK flip-flop. What is meant by race around condition? | (10) |
| 13 | Design a mod-11 asynchronous counter using T flip flops and discuss its disadvantages. | (10) |

- 14 Design a 4 bit Carry look ahead adder. (10)

PART D

Answer any two questions, each carries 10 marks

- 15 Design a counter to a given count sequence using T Flip flops 1, 2, 4, 6, 0, 5, 1,..... (10)
- 16 Design a Flash type 2-bit ADC. What is the difficulty in designing ADCs of higher order bits? (10)
- 17 a) Implement a half adder using VHDL. (3)
- b) Prepare the state table and excitation table for the Sequential machine shown below. Use T flip flop. (7)

