

D 30949

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Name.....

Reg. No.....

**FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION  
OCTOBER 2012.**

EC 09 501—DIGITAL SIGNAL PROCESSING

(2009 scheme)

Time : Three Hours

Maximum : 70 Marks

**Part A**

*Answer all questions.*

Short answer questions :

1. Write the Linearity Property of Discrete Fourier series.
2. Compute the Linear convolution of the two sequences  $x_1(n) = \{1, 1, 2, 2\}$  and  $x_2(n) = \{1, 2, 3, 4\}$ .
3. What is meant by limit cycle oscillation ?
4. Write the Blackmann window function.
5. What is meant by pipelining ?

(5 × 2 = 10 marks)

**Part B**

*Answer any four questions.*

1. State and prove associative law of convolution.
2. Compute the DFTs of the sequence  $x(n) = \cos \frac{n\pi}{2}$ , where  $N = 4$ , using Decimation in Frequency FFT algorithm.
3. Explain limit cycle behaviour of filter.
4. A digital system is characterized by the difference equation  $y(n) = 0.9y(n-1) + x(n)$  with  $x(n) = 0$  and initial condition  $y(-1) = 12$ . Determine the deadband of the system.
5. Compare bilinear transformation with other transformations based on their stability.
6. Explain the working of multiplier in Harvard architecture.

(4 × 5 = 20 marks)

**Part C**

1. Find the convolution of the two signals  $x(n) = u(n)$  and  $h(n) = a^n u(n)$ , ROC:  $|\hat{a}| < 1; n \geq 0$ .

Or.

2. Given :

$$X(k) = \{20, -5.828 - j 2.414, 0, -0.172 + j 0.414, 0, -0.172 + j, 0.414, 0, -5.282 + j 2.414\}$$

find  $x(n)$  using IFFT.

Turn over

3. Draw the Direct form I and Direct form II structures of :

$$H(z) = \frac{3 + 5z^{-1} - 8z^{-2} + 4z^{-5}}{2 + 3z^{-1} + 6z^{-3}}$$

Or

4. Develop the cascade and parallel forms for the transfer function :

$$H(z) = \frac{8z^3 - 4z^2 + 11z - 2}{(z - \frac{1}{4})(z^2 - z + \frac{1}{2})}$$

5. What is an optimal linear phase filter ? What parameters are optimized in these filters ? Explain.

Or

6. Explain analog frequency transformation and write the transformation formulae for LPF, HPF, BPF and band stop filter.
7. What are the main limitations of shared memory architectures ? Discuss different approaches in overcoming or reducing these limitations.

Or

8. Explain scheduling of inner loops in FFT processors.

(4 × 10 = 40 marks)

