MODULE II

Topic	Question	mark	Month &Year	Regulation
Number systems	Convert the hexadecimal number F3A7C2 to binary	2	Oct 11	2009
	Determine the value of the base x if $(211)_x=(158)_8$	5	Dec 10	2009
	Convert the following hexadecimal numbers into i)Octal and ii)Decimal i. 0.BC9 ii. 7FE.D53	5	Dec 10	2K
	Convert the following octal numbers into hexadecimal and Decimal i. 0.7345 ii. 4125.316	5	Dec 09	
	Convert the hexadecimal 2AC5 to decimal, octal and binary	5	Dec 05	
Binary codes	Write a short note on ASCII code	5	Jun 10	2004
	Write a short note on ASCII character code	5	Dec 08	
	Design a circuit that generates the 9's compliment of a BCD digit	15	Dec 08	
	Construct BCD to excess-3 code converter	5 15 15	Dec 07 Dec 07 Dec 08	2004 2K 2K
	Write a short note on Excess-3 code and gray code	5 5	Jun 07 Jun 07	2004 2K
	Give the significance of Gray code	2 5 5	Dec 10 Dec 11 Dec 07	2009 2K 2K
	Design a combinational circuit that converts a BCD to Gray code	15	Dec 09	2K
	Design a combinational circuit that converts a decimal digit from the BCD code to excess-3 code	15 15	Jun 09 Dec 06	
	Determine the binary code for each of the ten decimal digit using weighted code with weights 7,4,2 and 1	5	Dec 07	
Number representations	Perform 1010100-1000011 using 1's compliment and 2's compliments	2	Oct 12	2009
	Compare 1's complement and 2's compliment arithmetic	5	Jul 12	2004
	With an example, explain the fixed point and floating point representation	10	Jul 12	
	Perform the following subtraction using 2's complement representation i. $25_{10}-12_{10}$ ii. $16_{10}-8_{10}$	5	Dec 10	
	explain floating point representation	5	Jun 10,dec 07	
	Draw the circuit diagram of 4-bit multiplier using combination logic and explain its operation	15 15	Dec 11 Dec 10	2K
Adders &subtractors	Draw the logic diagrams of a look ahead carry generator and 4-bit full adder with look ahead carry and explain the operations	10	Oct 12	2009
	What are universal gates? Construct full adder and half adder using only the universal gates	10	Dec 10	
	Design a Half Adder and Half Subtractor	5	Jul 12	2004

		5	Jun 09	2K
	Design a full adder and realize using only NAND logic	10	Jun 10	2004
	Draw the block diagram of fast adder and explain	5	Jun 09	
	Explain unsigned adder and subtractor circuit	5	Jun 08	
	Explain the signed adder with circuit diagram	5	Dec 08	
	Draw the block diagram of 4-bit carry look ahead adder and explain its operation	10 15 15	Oct 11 Jun 08 Jun 09	2009 2004 2K
	Explain the principle of BCD adder with neat diagram	5 15 15 15 15 15 15	Dec 10 Dec 11 Dec 09 Dec 08 Dec 07 Jun 07 Dec 05	2009 2004 2004 2K 2K 2K 2K
	Draw the circuit of half Subtractor and explain	5	Dec 10	
	Construct a full subtractor	5	Dec 08	
	Construct a full adder	5 5	Jun 08 Dec 06	2K
	Write the concept of carry look ahead adder	5	Jun 07	
	Design a full Subtractor using NAND only	8	Dec 06	
	Construct a full adder with two half adder	5	Dec 05	
Mux and Demux	Implement F(A,B,C)=∑m(1,2,4,5) with a multiplexer	5	Oct 12	
	Draw the logic diagram of 4x1 multiplexer	5	Oct 11	2009
	Implement F(A,B,C)=∑m(1,3,5,6) with a multiplexer	5	Dec 10	
	Draw and explain 1 of 8 multiplexer	5	Dec 08	2004
	Explain the basic principle of multiplexers and Demultiplexer	15 15	Jun 07 Dec 05	2004 2K
	Implement a full adder with a multiplexer	15 15	Dec 11 Dec 07	
	Realize 8:1 multiplexer using two 4:1 multiplexer and explain	5 5	Dec 11 Dec 10	
	Implement the following function with an 8:1 multiplexer F(A,B,C,D)=∑m(0,1,3,4,8,9,15)	9 5	Dec 10 Jun 08	2K
	Draw and explain 1 to 8 Demultiplexer	5	Dec 09	
	Derive 1 of 16 multiplexer and explain	8	Jun 09	
	Draw 8:1 multiplexer using NAND only and explain	5	Dec 06	
Encoder &Decoder	Implement a full adder using suitable decoder and a logic gate.	5	Jul 12	
	Show how the function Y(A,B,C) = ∑m(0,2,3,4,5,7) can be implemented using 3 to 8 binary decoder and an OR gate.	10	Dec 08	2004
	Write the concept of encoder	5	Dec 07	
	A combinational circuit is defined by the following three functions $F_1 = \bar{x}\bar{y} + xy\,\bar{z}$ $F_2 = \bar{x} + y$ $F_3 = xy + \bar{x}\bar{y}$ Design the circuit with decoder and external gate	15	Dec 09	2K
	Draw the logic circuit for decimal to BCD encoder and explain	15		2K

	Write the concept of encoder and Decoder	5 15 15	Dec 10 Dec 08 Jun 08	2009 2K 2K
IC characteristics, TTL and ECL family	Explain the working of i) TTL NAND gate and ii) ECL gate with neat diagrams	10	Oct 12	2009
	Explain the operation of a TTL NAND gate with open collector output	10	Jul 12	2004
	Write a note on TTL interfacing	5	Jul 12	
	Define the following terms i. Noise margin ii. Propagation delay iii. Power dissipation	5	Dec 10	
	Draw and explain the operation of a two input TTL NAND gate	15 5	Dec 10 Oct 11	2004 2009
	What is meant by fan-in and fan-out	5 5 5 7	Jun 10 Jun 09 Jun 08 Dec 06	2004 2K 2K 2K
	Explain what is meant by noise immunity of digital IC?	5	Jun 09	2004
	Draw the circuit of an ECL logic for OR gate and explain its operation	15	Jun 09	
	List the characteristics of digital ICs	5 5	Jun 08 Jun 09	2004 2K
	Define fan-in, fan-out, noise margin in logic families	5	Jun 04	2K
	Discuss the operation of open collector TTL gate	15 15	Dec 11 Dec 07	2K
	Draw the circuit of an ECL logic for NOR gate and explain its operation	15 15	Dec 11 Dec 10	
	What are the advantages of TTL logic	5	Dec 10	
	Draw the circuit diagram ofSchottky TTL NAND gate and explain its operation. What are the advantages of TTL gate	15	Dec 09	
	Draw the circuit diagram ofa high speed TTL NAND and explain its operation	15	Jun 09	
	Define propagation delay and noise margin	5	Dec 08	
	Discuss the principle of ECL with neat circuit diagram	10 15	Oct 11 Dec 08	2009 2K
	Explain the operation of ECL	15 15 15	Jun 08 Dec 05 Jun 04	2K
	Explain the principle of Schottky TTL with neat circuit diagram	10 15 15	Dec 10 Jun 07 Dec 05	2009 2K 2K
	Explain the principle of TTL logic family	15	Jun 04	2K