MODULE IV

Topic	Question	mark	Month &Year	Regulation
Finite state machine(FSM), State diagram, State table, Mealy and Moore type machine	What is Mealy and Moore model	5	Oct 11	2009
	What is meant by state diagram	5 5	Jun 07 Dec 06	2K 2K
	Give examples of state diagram	5	Dec 08	2K
	Derive the state table of the following sequential circuit	5	Dec 06	2K
	With suitable examples explain the difference between Mealy and Moore state models	6	Jul 12	2004
	Discuss the concept of Mealy and Moore models	15	Dec 07	2004
	State the difference between Mealy and Moore state models	5 5	Dec 10 Jun 09	2004 2004
	Explain the concept of More models	5 5	Jun 10 Dec 08	2004 2004
	Explain about Mealy state model	5	Jun 08	2004
Design of synchronous counters And sequence generators	Design a counter with the following repeated binary sequence 0,1,2,4,6.use D flip flop	5	Oct 11	2009
	Construct MOD 10 counter Construct MOD 12 counter	5 5	Oct 11 Dec 10	2009 2009
	Design a sequential circuit with two JK flip flop A and B and two inputs E and x. If E=0 the state of the circuit remains same state regardless of the value of x. When E=1 and x=1 the circuit goes through the state transition from 00 to 01 to 10 to 11 back to 00 and repeat. When E=1 and x=0 the circuit goes through the state transition from 00 to 11 to 10 to 01 back to 00 and repeat.	10 15	Dec 10 Jun 08	2009 2K
	Design a sequential circuit with two D flip flop A and B and one inputx. When x=0 the state of the circuit remains same When x=1, the circuit goes through the state transition from 00 to 01 to 11 to 10 back to 00 and repeat.	15 15	Dec 05 Jun 04	2K 2K
	Design a counter with the following repeated binary sequence 0,1,3,7,6,4 using T flip flop	10 15	Dec 10 Dec 09	2009 2K

Design of synchronous counters And sequence generators	Design a counter with the following repeated binary sequence 0,1,3,7,6,4 using D flip flop	15	Jun 04	2K
	Design a counter with the following repeated binary sequence using T flip flop i) 0,1,2,3,5,6 ii) 0,1,3,7,6,4	15	Oct 12	2009
	Design a counter with the following binary sequence 0,4,2,1,6 and repeat .use JK flip flop	15 15	Jun 10 Dec 10	2004 2K
	Design a counter with the following binary sequence 0, 1,3,2,6, 4, 5, 7 and repeat.	15	Jun 09	2K
	Design a counter with the following repeated binary sequence 0,1, 2,3,4,5,6 using JK flip flop	15	Dec 07	2K
	Draw the circuit of 4 bit synchronous counter using JK flip-flop and explain its operation with truth table	15	Jun 09	2004
	Design a counter that counts pulses on line W and displays the count in the sequence 0, 2, 1, 3, 0, 2… Use D flip flop in your circuit	15	Dec 08	2004
	Design a counter that counts pulses on line W and displays the count in the sequence 1, 3, 7, 4, 1, 3, 7… Use JK flip flop in your circuit	15	Jun 08	2004
	Construct MOD 12 counter using JK flip flop	15	Dec 07	2004
	Design a sequential circuit to generate the following repeated random sequence 1, 3, 7, 2, 5, 1, 3……	15	Dec 06	2K
	Design a sequential circuit with two flip flop and one external input x for the following conditions i) When x=0 the state of the circuit remains same ii) When x=1, the circuit goes through the state transition from 0 to 1 to 4 to 3 to 2 back to 0 and repeat. Use JK flip flop	15	Dec 10	2K
Design of sequence detectors	Derive the state diagram for an FSM that has an input **W** and an output **Z**. The machine has to generate **Z**=1 when the previous four values of **W** were 1001 or 1111 otherwise **Z**=0. Overlapping input patterns are allowed	15	Jun 10	2004
Design of simple synchronous machine	Design a sequential parity detector and explain its operation	9	Jul 12	2004
	A sequential circuit has three flip-flop A, B, C; one input x and one output y. The state diagram is given in figure (1).The circuit is to be designed by treating the unused states as don't care conditions. i) Use D flip flops in the design ii) Use JK flip flop in the design	10	Oct 12	2009

<table>
<tr><td rowspan="4">Design of simple synchronous machine</td><td></td><td></td><td></td><td></td></tr>
<tr><td>Explain the design of simple synchronous machine with example</td><td>6</td><td>Oct 11</td><td>2009</td></tr>
<tr><td>Design a sequential serial adder using i) Mealy state model
ii) Moore state model</td><td>15</td><td>Dec 10</td><td>2004</td></tr>
<tr><td>Derive a circuit that realizes the FSM defined by the state assigned table in the following table using JK flip flop

<table>
<tr><th rowspan="2">Present state
y_2y_1</th><th colspan="2">Next state</th><th rowspan="2">Output
Z</th></tr>
<tr><th>W=0
Y_2Y_1</th><th>W=1
Y_2Y_1</th></tr>
<tr><td>0 0
0 1
1 0
1 1</td><td>1 0
0 1
1 1
1 0</td><td>1 1
0 0
0 0
0 1</td><td>0
0
0
1</td></tr>
</table></td><td>15</td><td>Dec 08</td><td>2004</td></tr>
<tr><td rowspan="5">state minimization</td><td>Explain the partitioning procedure for state minimization with suitable example</td><td>15</td><td>Dec 12</td><td>2004</td></tr>
<tr><td>Derive a minimal state table for a single input single output Moore type FSM that produces output logic ‘1’, if in the input sequence it detects either 110 or 101 patterns. Overlapping sequence should detected</td><td>15</td><td>Jun 09</td><td>2004</td></tr>
<tr><td>Reduce the number of states in the following state table and tabulate the reduced state table

<table>
<tr><th rowspan="2">Present state</th><th colspan="2">Next state</th><th colspan="2">Output</th></tr>
<tr><th>x=0</th><th>x=1</th><th>x=0</th><th>x=1</th></tr>
<tr><td>a
b
c
d
e
f
g
h</td><td>f
d
f
g
d
f
g
g</td><td>b
c
e
a
c
b
h
a</td><td>0
0
0
1
0
1
0
1</td><td>0
0
0
0
0
1
1
0</td></tr>
</table></td><td>5</td><td>Dec 10</td><td>2K</td></tr>
<tr><td>Discuss the state table reduction technique

Discuss the state table reduction technique
Discuss the state diagram reduction procedure with an example</td><td>15
15
15
15
15</td><td>Jun 07
Dec 08
Dec 07
Jun 08
Dec 05</td><td>2K
2K
2K
2K
2K</td></tr>
<tr><td></td><td>Write the importance of ASM chart with example</td><td>5</td><td>Oct 12</td><td>2009</td></tr>
</table>

ASM chart	What is the need for an ASM chart? Compare it with a state diagram	5	Jul 12	2004
	What are the basic building blocks of an ASM chart? Explain	5	Dec 10	2004
	Draw the state boxes used in ASM chart	5	Dec 07	2004
	Explain how ASM chart differs from a conventional flowchart	4	Oct 11	2009
	Write the application of ASM chart	5	Dec 10	2009
ASM chart	Draw the ASM chart for the following state diagram and design the circuit.	5	Jul 12	2004