MODULE II

Topic	Question	mark	Month &Year	Regulation
MEMORY TECHNOLOGY (Characteristics, ROM, RAM, SAM)	Define Memory Density and Memory Access time	2	Apr 12	2009
	With the conceptual model diagram, explain the random access memory	5	Jun 11	2009
	Write a note on Random Access Memories	5	Apr 13	2009
	State Kerr effect	2	Jun 11	2009
	Write a short note on read only memories	5	Dec 07	2004
	Write a short note on device characteristics	5	Dec 08	2004
	Explain the various characteristics of memory devices	15	Dec 10	2004
	Describe about memory organization	15	Jun 08	2004
MULTI LEVEL MEMORIES (Physical memory,Virtual memory,Address translation, Cache,Address mapping)	Write a short note on memory systems	5	Dec 08	2004
	Write a note on multilevel memories	5	Apr 12	2009
	Discuss in detail about the common memory hierarchies with two, three and four levels	10	Jun 11	2009
	Draw the common memory hierarchies and give a brief explanation about them	5	Dec 10	2004
	Describe the virtual memory address translation technique	15	Dec 08	2004
	Design an intelligent page transfer scheme between a cache memory and main storage having following specifications i) 4 word cache page, each word of 4 bytes ii) Bus width of 32 bits and bus transfer time of 50n sec iii) 4 module main storage with cycle time of 200n sec Give the timing diagram for write back transfer scheme	15	Jun 09	2004
	A virtual memory system has 16K word logical address space, 8K word physical address space with page size of 2K words. The page address trace of a program has been found to be 7 5 3 2 1 6 4 1 6 7 4 2 0 1 3 5 Note the four pages resident in the memory after each page reference change for each of the following replacement policies i) FIFO ii) LRU iii) Anticipatory swapping	15	Jun 09	2004
	Write a note on virtual and cache memories	5	Apr 12	2009
	What is a cache memory	2	Apr 13	2009

Prepared by:- Susan Varghese, Asst Prof. ECE dept

Cache and address mapping	Explain the advantage of cache memory	5	Jun 08	2004
	With block diagram explain the processor memory communication with and without a cache memory	5	Jun 11	2009
	Discuss the various mapping schemes used in cache design. Compare them	10	Apr 13	2009
	Discuss in detail about Associative and set associative addressing modes	10	Jun 11	2009
	Explain the use of associative memory for increasing the access rate	5	Dec07	2004
	What is the need for a cache memory? Explain three types of memory mapping followed in the cache memory.	15 15	Dec 07 Jun08	2004 2004
	With neat diagram, explain the direct mapped cache and associative mapped cache	15	Dec 08	2004
	Explain the design of 256KB of direct mapped cache for a microprocessor	15	Dec 10	2004
	Write the general approach used to design the caches main size parameters $K_1 S_1 P_1$	5	Dec 10	2004
	Organize the subfields of MAR to realize a block set associatively mapped cache main storage hierarchical memory with MS capacity of 16K pages of 16 words each and the cache capacity of 256 pages divided into sets, each set having 8 pages.	5	Jun 09	2004
	A set associative mapping cache has a set size of 4. The cache capacity is 2K words and that of main storage is 128K x 32. Derive all information required to design the cache memory and note the data path for the set associative organization. Determine the average memory access time for the cache hit ratio of 0.85 cache access time of 100n sec and main memory access time of 500n sec.	5	Jun 09	2004